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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/620,862	07/15/2003	H. Peter Anvin	TRAN-P082	9139

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WAGNER, MURABITO & HAO LLP
Third Floor
Two North Market Street
San Jose, CA 95113

EXAMINER	
GEIB, BENJAMIN P	
ART UNIT	PAPER NUMBER
2181	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/07/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/620,862	ANVIN ET AL.	
	Examiner	Art Unit	
	Benjamin P. Geib	2181	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 November 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1-26 have been examined.

2. It is hereby acknowledged that the following papers have been received and placed of record in the file: request for continued examination on 11/09/2006.

3. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 11/09/2006 has been entered.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. Claims 2, 3, 11, 12, 20, and 21 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention. More specifically, the above-mentioned claims recite the limitation "operations that involve memory other than microprocessor registers that is private to a microprocessor". The Examiner has found no support in the specification for such a limitation. The

memory that is private to a microprocessor described in the specification is microprocessor registers (See specification page 6, line 24 – page 7, line 6; Fig. 1 or 2, component 102). In the remarks section of the Applicant's Amendment received on 05/19/2006, the Applicant cites page 7, lines 5-6, as having support for the amendment of "other than microprocessor registers" to the above-cited limitation. The cited lines state that "there can be instances of private memory other than or in addition to CPU register 102". This statement, while indicating that there may instances of private memory other than a specific register (i.e. CPU register 102), does not enable one skilled in the art to make and use "operations that involve memory other than microprocessor registers that is private to a microprocessor".

6. Claims 2, 3, 11, 12, 20, and 21 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. More specifically, the above-mentioned claims recite the limitation "operations that involve memory other than microprocessor registers that is private to a microprocessor". The Examiner has found no support in the specification for such a limitation. The memory that is private to a microprocessor described in the specification is microprocessor registers (See specification page 6, line 24 – page 7, line 6; Fig. 1 or 2, component 102). In the remarks section of the Applicant's Amendment received on 05/19/2006, the

Applicant cites page 7, lines 5-6, as having support for the amendment of "other than microprocessor registers" to the above-cited limitation. The cited lines state that "there can be instances of private memory other than or in addition to CPU register 102". This statement, while indicating that there may instances of private memory other than a specific register (i.e. CPU register 102), does not reasonably convey to one skilled in the art that the inventor(s) has possession of "operations that involve memory other than microprocessor registers that is private to a microprocessor".

Claim Rejections - 35 USC § 102

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

8. Claims 1, 4-8, 19, and 22-25 are rejected under 35 U.S.C. 102(e) as being anticipated by Dice, U.S. Patent No. 6,854,048.

9. Referring to claim 1, Dice has taught a method providing partial speculative operation in lieu of suspending speculation, said method comprising:

operating in a first mode of speculative operation *[when the speculation indicator is set to indicate that speculation is allowed on load instructions]*, said first mode permitting speculation of a first set of speculative operations *[speculation is permitted of all instructions] [column 12, lines 1-15]*;

experiencing an event *[the setting of the speculation indicator to indicate that speculation is not allowed on load instructions]* during said operating *[column 12, line 64 – column 13, line 15]*;

suspending a non-null first subset *[load instructions]* of said first set of speculative operations, wherein speculative operations in said first subset are not permitted during said suspending *[load instructions are not permitted to execute speculatively; column 12, line 64 – column 13, line 15]*; and

exiting said first mode and entering a second mode of speculative operation *[when the speculation indicator is set to indicate that speculation is not allowed on load instructions; column 12, lines 1-15]* in response to said event, said second mode permitting speculation of a non-null second subset *[all instructions except load instructions]* of said first set, wherein said second subset comprises speculative operations not in said first subset *[column 12, line 64 – column 13, line 15]*.

10. Referring to claim 4, Dice has taught the method of Claim 1 wherein said second subset comprises speculative operations that are invisible external to a microprocessor *[instructions that operate on memory internal to the processor; column 12, line 64 – column 13, line 15]*.

11. Referring to claim 5, Dice has taught the method of Claim 1 wherein said event is selected from the group consisting of a fault, a direct memory access request, and an I/O read *[the set si instruction is an I/O read; column 12, lines 36-42]*.

12. Referring to claim 6, Dice has taught the method of Claim 1 further comprising suspending speculative operation in response to a second event *[a read-after-write hazard; column 16, lines 5-14]*.

13. Referring to claim 7, Dice has taught the method of Claim 1 further comprising returning to said first mode after said event is handled *[column 13, lines 16-21]*.

14. Referring to claim 8, Dice has taught counting the number of instructions executed in said first mode prior to said event and returning to said first mode upon executing the same number of instructions after entering said second mode [column 16, lines 5-14].

15. Referring to claim 19, Dice has taught a computer system comprising:

a main memory *[FIG. 4, component 110; column 14, lines 51-67]*; and

a microprocessor coupled to said main memory *[FIG. 4, component 120; column 14, lines 32-50]*;

wherein said computer system implements a first mode of speculative operation *[when the speculation indicator is set to indicate that speculation is allowed on load instructions; column 15, lines 20-33]*, a second mode of partial speculative operation *[when the speculation indicator is set to indicate that speculation is not allowed on load instructions; column 15, lines 20-33]*, and a

third mode in which speculative operations are suspended in entirety *[when recovering from a read-after-write hazard; column 16, 5-14]*.

16. Referring to claim 22, given the similarities between claim 4 and claim 22 the arguments as stated for the rejection of claim 4 also apply to claim 22.

17. Referring to claim 23, given the similarities between claim 5 and claim 23 the arguments as stated for the rejection of claim 5 also apply to claim 23.

18. Referring to claim 24, given the similarities between claim 6 and claim 24 the arguments as stated for the rejection of claim 6 also apply to claim 24.

19. Referring to claim 25, given the similarities between claim 7 and claim 25 the arguments as stated for the rejection of claim 7 also apply to claim 25.

Claim Rejections - 35 USC § 103

20. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

21. Claims 2, 3, 20, and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dice.

22. Referring to claim 2, Dice has taught the method of Claim 1 wherein said first set of speculative operations comprises all operations *[column 12, lines 1-15]*, but is silent on what types of operations exist.

However, the Examiner takes Official Notice that microprocessor register operations, operations that involve memory other than microprocessor registers that is private to a microprocessor, input/output (I/O) writes, main memory reads, main memory writes, and non-architectural faults are conventional and well-known operations.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Dice to include microprocessor register operations, operations that involve memory other than microprocessor registers that is private to a microprocessor, input/output (I/O) writes, main memory reads, main memory writes, and non-architectural faults.

The suggestion/motivation for doing so would have been that the types of operations existent would be disclosed, thereby realizing the systems functionality.

23. Referring to claim 3, Dice has taught the method of Claim 1 wherein said second subset comprises all operations except load instructions *[column 12, line 64 – column 13, line 15]*, but is silent on the types of operations executed.

However, the Examiner takes Official Notice that microprocessor register operations, operations that involve memory other than microprocessor registers that is private to a microprocessor, and architectural faults are conventional and well-known operations.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Dice to include microprocessor register operations,

operations that involve memory other than microprocessor registers that is private to a microprocessor, and architectural faults.

The suggestion/motivation for doing so would have been that the types of operations existent would be disclosed, thereby realizing the systems functionality.

24. Referring to claim 20, given the similarities between claim 2 and claim 20 the arguments as stated for the rejection of claim 2 also apply to claim 20.

25. Referring to claim 21, given the similarities between claim 3 and claim 21 the arguments as stated for the rejection of claim 3 also apply to claim 21.

26. Claims 9 and 26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dice in view of Dehnert et al., "The Transmeta Code Morphing Software: Using Speculation, Recovery, and Adaptive Retranslation to Address Real-Life Challenges" (Herein referred to as Dehnert).

27. Referring to claim 9, Dice has taught the method of Claim 1 implemented using a microprocessor comprising host hardware *(Dice; column 10, lines 42-65)*.

Dice does not disclose expressly that the microprocessor additionally comprises translation software, said translation software running directly on said host hardware, said translation software for interpreting and translating a sequence of non-native instructions into a sequence of native instructions, wherein said interpreting is permitted during said second mode.

Dehnert discloses a microprocessor *(Transmeta Crusoe microprocessor)* comprising a combination of translation software *(Code Morphing Software (CMS); See Fig. 1)* and host hardware *(VLIW processor; See second paragraph of section labeled "Crusoe and CMS" on page 2)*, said translation software running directly on said host hardware, said translation software for interpreting and translating a sequence of non-native instructions *(x86 instructions)* into a sequence of native instructions (VLIW instruction "molecule") *(Dehnert; See section labeled "Crusoe and CMS" on pages 2-3).*

At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to modify the microprocessor of Dice to include translation software that interprets and translates a sequence of non-native instructions into a sequence of native instructions as taught by Dehnert. In doing so, said interpreting would be permitted during said second mode.

The suggestion/motivation for doing so would have been that translation software allows the native instruction set to be modified while the microprocessor advantageously remains compatible with programs written using the non-native instructions *(Dehnert; See section labeled "Crusoe and CMS" on pages 2-3).*

28. Referring to claim 26, given the similarities between claim 9 and claim 26 the arguments as stated for the rejection of claim 9 also apply to claim 26.

29. Claims 10-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dehnert in view of Dice.

30. Referring to claim 10, Dehnert has taught a method providing partial speculative operation, said method comprising:

executing forward from a speculation boundary *[start of a translation]* representing a memory state *[shadow register state]*, said executing according to a full speculation mode that permits a set of speculative operations *[See section 3.1 on pages 3-4]*;

experiencing an event *[exception]* during said executing *[See section 3.1 on pages 12-13]*;

rolling back to said speculation boundary *[start of a translation]* and restoring said memory state *[shadow register state]* in response to said event *[See section 3.1 on pages 3-4]*; and

executing forward from said speculation boundary non-speculatively *[Execution from speculation boundary is done in-order and therefore non-speculatively; See section 3.1 on pages 3-4]*

Dehnert does not disclose expressly suspending a non-null first subset of said set of speculative operations; wherein said first subset does not include all of said speculative operations and wherein speculative operations in said first subset are not permitted during said suspending. Dehnert further does not disclose expressly that executing forward from said speculation boundary is done according to a partial speculation mode that permits a non-null subset of said set of speculative operations, wherein said second subset comprises speculative operations not in said first subset and wherein said partial speculation mode is used in lieu of suspending said set of speculative operations in entirety.

Dice has taught suspending a non-null first subset *[Dice; load instructions]* of said set of speculative operations, wherein said first subset does not include all of said speculative operations and wherein speculative operations in said first subset are not permitted during said suspending *[Dice; load instructions are not permitted to execute speculatively; column 12, line 64 – column 13, line 15]*. Dice has further taught executing according to a partial speculation mode *[Dice; when the speculation indicator is set to indicate that speculation is not allowed on load instructions; column 12, lines 1-15]* that permits a non-null second subset *[Dice; all instructions except load instructions]* of said set of speculative operations, wherein said second subset comprises speculative operations not in said first subset and wherein said partial speculation mode is used in lieu of suspending said set of speculative operations in entirety *[Dice; column 12, line 64 – column 13, line 15]*.

At the time the invention was made, it would have been obvious to a person of ordinary skill in the art to modify the system of Dehnert to suspend a non-null first subset of said set of speculative operations, wherein said first subset does not include all of said speculative operations and wherein speculative operations in said first subset are not permitted during said suspending as taught by Dice. It would further have been obvious to modify the system of Dehnert to execute forward from said speculation boundary according to a partial speculation mode that permits a non-null subset of said set of speculative operations, wherein said second subset comprises speculative operations not in said first subset and wherein said partial speculation mode is

used in lieu of suspending said set of speculative operations in entirety as taught by Dice.

The suggestion/motivation for doing so would have been that an extremely fine level of control over when speculative execution is permitted is provided *[Dice; column 6, lines 6-28]*.

31. Referring to claim 11, Dehnert and Dice have taught the method of Claim 10 wherein said set of speculative operations comprises microprocessor register operations *[Dehnert; Since registers are shadowed, register operations must execute speculatively; see second paragraph of section 3.1]*, operations that involve memory that is private to a microprocessor *[Dehner; Registers are memory that is private to the microprocessor. Therefore, register operations involve memory that is private to the microprocessor]*, input/output (I/O) writes *[Dehnert; see fourth paragraph of section 3.4]*, main memory reads *[Dehnert; see second paragraph of section 3]*, main memory writes *[Dehnert; see second paragraph of section 3]*, and non-architectural faults *[Dehnert; faults (i.e. errors) that are not genuine; see section 3.2]*.

Dehnert and Dice have not explicitly taught that the operations that involve memory that is private to a microprocessor involve memory other than microprocessor registers.

However, the Examiner takes Official Notice that the use of an instruction cache in a microprocessor is conventional and well-known.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the microprocessor of Dehnert and Dice to include

an instruction cache. An instruction cache is memory that is private to a microprocessor. Operations (i.e. instructions) that are stored in the instruction cache are operations that involve memory other than microprocessor registers that is private to a microprocessor.

The suggestion/motivation for doing so would have been that the time required to fetch instructions is advantageously decreased.

32. Referring to claim 12, Dehnert and Dice have taught the method of Claim 10 wherein said second subset comprises microprocessor register operations *[Dehnert; Since registers are shadowed, register operations must execute speculatively; see second paragraph of section 3.1]*, operations that involve memory that is private to a microprocessor *[Dehner; Registers are memory that is private to the microprocessor. Therefore, register operations involve memory that is private to the microprocessor]*, and architectural faults *[Dehnert; faults (i.e. errors); see section 3.2].*

Dehnert and Dice have not explicitly taught that the operations that involve memory that is private to a microprocessor involve memory other than microprocessor registers.

However, the Examiner takes Official Notice that the use of an instruction cache in a microprocessor is conventional and well-known.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the microprocessor of Dehnert and Dice to include an instruction cache. An instruction cache is memory that is private to a microprocessor. Operations (i.e. instructions) that are stored in the instruction

cache are operations that involve memory other than microprocessor registers that is private to a microprocessor.

The suggestion/motivation for doing so would have been that the time required to fetch instructions is advantageously decreased.

33. Referring to claim 13, Dehnert and Dice have taught the method of Claim 10 wherein said second subset of speculative operations comprises speculative memory operations that are invisible external to a microprocessor *[Dehnert; register operations; 2nd paragraph of section 3.1]*.

34. Referring to claim 14, Dehnert and Dice have taught the method of Claim 10 wherein said event is selected from the group consisting of a fault *[Dehnert; see section 3.2]*, a direct memory access request, and an I/O read.

35. Referring to claim 15, Dehnert and Dice have taught the method of Claim 10 further comprising:

detecting a second event during operation in said partial speculation mode *[Dice; a read-after-write hazard]*; and suspending speculative operation in response to said second event *[Dice; column 16, lines 5-14]*.

36. Referring to claim 16, Dehnert and Dice have taught the method of Claim 10 further comprising:

handling said event; and returning to said full speculation mode after said event is handled *[Dice; column 13, lines 16-21]*.

37. Referring to claim 17, Dehnert and Dice have taught the method of Claim 10 further comprising:

counting the number of instructions executed in said full speculation mode prior to said event *[The number of instructions is counted using the program counter, which is inherently needed to correctly execute the program]*;

executing the same number of instructions after entering said partial speculation mode *[Dehnert; The instructions corresponding to the faulting translation are executed. Therefore, at least the same number of instructions are executed; See section 3.1 on pages 3-4]*; and

returning to said full speculation mode after executing said same number of instructions *[Dehnert; See section 3.1 on pages 3-4]*.

38. Referring to claim 18, Dehnert and Dice have taught the method of Claim 10 implemented using a microprocessor comprising a combination of translation software and host hardware, said translation software running directly on said host hardware, said translation software for interpreting and translating a sequence of non-native instructions into a sequence of native instructions, wherein said interpreting is permitted during said partial speculation mode *[Dehnert; See section 2 on pages 2-3]*.

Response to Arguments

39. Applicant's arguments with respect to claims 1-26 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

40. The following is text cited from 37 CFR 1.111(c): In amending in reply to a rejection of claims in an application or patent under reexamination, the applicant or patent owner must clearly point out the patentable novelty which he or she thinks the claims present in view of the state of the art disclosed by the references cited or the objections made. The applicant or patent owner must also show how the amendments avoid such references or objections.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Benjamin P. Geib whose telephone number is (571) 272-8628. The examiner can normally be reached on Mon-Fri 8:30am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Donald Sparks can be reached on (571) 272-4201. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Benjamin P Geib
Examiner
Art Unit 2181

DONALD SPARKS
SUPERVISORY PATENT EXAMINER